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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,498	09/14/2000	Alnoor M. Shivji	005100.P004	8758

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BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 GATEHOUSE ROAD
SUITE 100 EAST
FALLS CHURCH, VA 22042-1248

EXAMINER	
NGUYEN, STEVEN H D	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/661,498	SHIVJI ET AL.	
	Examiner	Art Unit	
	Steven HD Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1, 7 and 11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 7 of U.S. Patent No. 6834049. Although the conflicting claims are not identical, they are not patentably distinct from each other because the applicant merely broaden the scope of the patented claims by not claims some elements (i.e I/O ports, queues etc). The application's claims are nearly identical in every other respect to the patent claims such as multiplexer, a latch, a space control register etc. Therefore, the applicant simply broader versions of the patent claims. It is the examiner's position that broadening the patented claims by not claiming some of claim elements of the patented claims would have been obvious to one of ordinary skill in the art in view of the patented claims. It is important to note that the instant application is a copending of the application that yielded the patent (US Pat 6834049) used herein as the basis for the obviousness type of double patenting rejection. The applicant is attempting to broaden the application's claims by eliminating some of the claim elements in the patent at issue here.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 11-12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Garg (US 2002/0131442).

Regarding claim 11, Garg discloses a method of receiving a bit stream of multiple bits streams (Fig 7, Ref 702 is multiplexer for receiving a multiple bits stream into an input of multiplexer which contains 32 channels "rails" wherein the signal have a format of STS-1) and selecting at least one bits from a stream of bits based, at least in part, on a space control register value and time control register value to output a output bits stream according to the format of output bit map (Fig 7, Ref 702 and 710 used to select at least one bit from the bit stream based one 5 bit rail selection value "space control register value" and 5 bit slot selection value "time control register value" to output an output bit stream having a second format according the output bit map of storage 706 which is different from the input bit stream of first format STS-1; Fig 7, Ref 706, the bit map of 706 inherently has a different format than the input format of the input stream).

Regarding claim 12, Garg discloses the space control register value indicating a selected stream of data from a plurality of streams of data (Fig 7, Ref 702 uses the input value of 5 bit rail selection for selecting the bits from the multiple bits stream for output to the latch 710).

Regarding claim 14, Garg discloses the time control register value indicating at least one bits from a selected stream of data (Fig 7, Ref 708 uses the input value of 5 bit slot selection for selecting the bits from selected stream for inputting into the latch 710).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7, 10, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garg (US 20020131442).

Regarding claim 1, Garg discloses a circuit comprising a multiplexer (Fig 7, Ref 702) which has an input for receiving space control register value to control the multiplexer (Fig 7, 5 bit rail selection) and receiving a bit stream having a first format form a plurality of multiple bit streams and a latch (Fig 7, Ref 710) coupled to receive a signal from the multiplexer and a control circuit coupled to control the latch, the control circuit to select at least one bits from stream of bits output by the multiplexer (Fig 7, Ref 708) for generating a second output stream having a second format according to the output bit map storage (Fig 7, Ref 706, the bit map of 706 inherently has a different format than the input format of the input stream). Garg does not fully disclose a space control register. However, it would have been obvious to one of ordinary skill in the art to apply a register for storing the value because it is well known and expected in the art to use a register to store a value for controlling a multiplexer.

Regarding claim 2-5, Garg does not disclose the multiplexer comprising a plurality of multiplexers such a first, second, third, four multiplexer are 8:1 and fifth multiplexer is 6:1 wherein the input of fifth multiplexer coupled to the output of first, second, third and four multiplexer. However, it would have been obvious to one of ordinary skill in the art to cascade four 8:1 multiplexer to one 6:1 multiplexer to obtain 32:1 multiplexer because it is well known and expected in the art to cascade the multiplexers. The motivation would have been to increase the input stream to the switch core.

Regarding claim 7, Garg discloses the control circuit comprising a time control register value for indicating a selected bit from a sequence of bits (Fig 7, Ref 5 bit slot selection) and a counter to count bits in the sequence of bits from a predetermined bit (Fig 7, Ref counter) and a comparator for comparing the value of the counter and the value of time control register for generating a load signal to enable the latch to store the value output by the multiplexer (Fig 7, Ref 708). However, Garg does not discloses the time control register for storing the value of time control register. Therefore, it would have been obvious to one of ordinary skill in the art to apply a register for storing the value because it is well known and expected in the art to use a register to store a value for using to compare with another value to generate an output value.

Regarding claim 10, Garg does not disclose the multiplexer receiving the logical values to generates alarm signal. However, Garg discloses a space and time switch for carrying the SONET signal that is implicitly disclosed the logical values for using to generate alarm signals.

Regarding claims 6, 13 and 15, Garg does not disclose the space/time control register value being programmable. However, it is would have been obvious to one of ordinary skill in the art to implement a value which is stored in the register to be programmable and

programmable register is well known and expected in the art. It is a designer choice. The motivation would have been to allow the manufacture to setup the value according to the network.

7. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garg in view of Irwin (USP 5841771).

Regarding claims 8-9, Garg discloses a second multiplexer for receiving a signal output by the latch (Fig 8, Ref 802) and a second control circuit to control the second multiplexer (Fig 8, Ref 10 bit control for selection which is received from a control circuit). However, Garg does not disclose a second multiplexer coupled to receive an output signal by another circuit and a second latch coupled to receive a signal output by the second multiplexer. In the same field of endeavor, Irwin discloses a second multiplexer coupled to receive an output signal by another circuit and a second latch coupled to receive a signal output by the second multiplexer (Fig 13, Ref 706 is a second multiplexer for receiving out signals from 703 and 615 and for coupling to second latch 617).

Since, Garg suggest the output of first latch is coupled to a second multiplexer having an input for receiving a output from control circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a second multiplexer coupled to receive an output signal by another circuit and a second latch coupled to receive a signal output by the second multiplexer as disclosed by Irwin into Garg's system. The motivation would have been to simultaneously read out the data from storage to reduce transmission delay.

Response to Arguments

8. Applicant's arguments filed 11/29/04 have been fully considered but they are not persuasive.

In response to pages 7-10, the applicant states that Garg fails to disclose a method and system for receiving a bit stream having a first format (768 bit of STS-1) at a multiplexer and using a control circuit for latching out the output from the multiplexing a second bit stream having a second format (32 X 24, output bit map read on second format "permutation from first format to second format") for switching purposed.

Conclusion

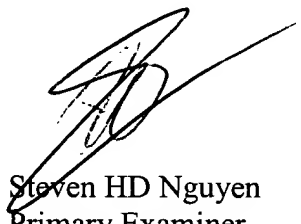
9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (571) 272-3159. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Steven HD Nguyen
Primary Examiner
Art Unit 2665
2/15/05